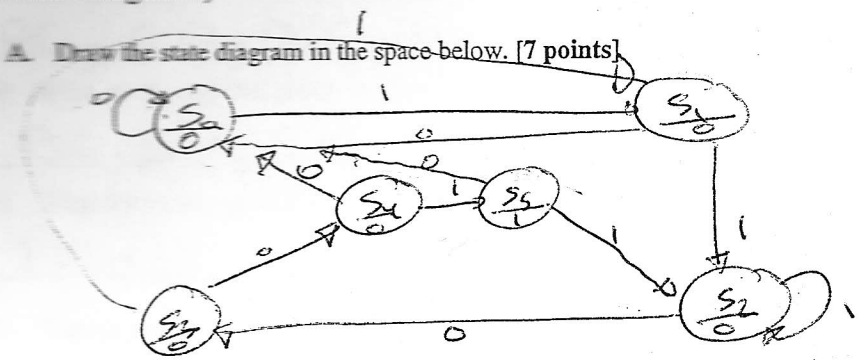
Problem 1: [10 points]

Using a Moore machine with D Flip-Flops, design a sequence detector that would output a Z=1 only after detecting the sequence 11001 on its single input X. Call the states S0, S1 etc. (use don't cares for illegal states and use simplest state assignment)

A. Draw the state diagram in the space below. **[7 points]**



B. Fill as much as needed in the corresponding state and transition tables shown below.

	X		
S	0	1	Z
S0	S0	S1	0
S1	S0	S2	0
S2	S3	S2	0
S3	S4	S1	0
S4	S0	S5	0
S5	S0	S2	1
	S*		

	X		
Q1Q2Q3	0	1	Z
000	000	001	0
001	000	010	0
010	011	010	0
011	100	001	0
100	000	101	0
101	000	010	1
	D1,D2,D3		

C. The excitation equations are given by: **[3 points]**

Q3X \ Q1Q2	00	01	11	10
00	0	0	d	0
01	0	0	d	1
11	0	0	d	0
10	0	1	d	0

D1 = $Q_1Q_3'X + Q_2Q_3X'$

Q3X \ Q1Q2	00	01	11	10
00	0	1	d	0
01	0	1	d	0
11	1	0	d	1
10	0	0	d	0

D2 = $Q_2'Q_3X + Q_2Q_3'$

Q3X \ Q1Q2	00	01	11	10
00	0	1	d	0
01	1	0	d	1
11	0	1	d	0
10	0	0	d	0

D3 = $Q_2'Q_3'X + Q_2Q_3X + Q_2Q$

ess. we look at (1) if its neighbors can g all together then its ess. prime

Problem 2: [10 points] 5

Consider the function: $F = \Sigma_{A,B,C,D}(0, 2, 3, 5, 7, 8, 10, 11, 14, 15)$

a) What are the prime implicants of F? [**2 points**]

AC, CD, B'C, A'BD, ~~B'C'D'~~, ~~A'B'D'~~, ~~AB'D'~~ B'D'

b) What are the essential prime implicants of F? [**2 points**]

AC, ~~CD~~, ~~B'C~~, A'BD, B'D'

c) What is a minimum SOP expression for F? [**3 points**]

AC + CD ~~+ B'C~~ + A'BD + B'D'

CD \ AB	00	01	11	10
00	1	0	[illegible]	1
01	0	1	0	0
11	1	1	1	1
10	1	0	1	1

d) What is a minimum POS expression for F? [**3 points**]

(B' + C + D) · (A' + C + D) · (B + C + D') · (A + B' + D) (A' + B' + C)

Problem 3: [10 points]

Consider the Boolean function $F = \Sigma_{A,B,C,D}(1, 3, 4, 11, 12, 13, 14, 15)$.

a) Implement F using a 4-input multiplexer and external gates. Connect A and B to the select lines. [**5 points**]

b) Implement F using two 3-to-8 decoders with enables, an inverter and OR gates with maximum inputs of 4. [**5 points**]

Problem 4: [10 points] 10

Design an Excess-3 to BCD code converter that gives output code of don't-cares for all invalid input combinations. Complete the table to include for every integer the corresponding BCD code representation.

EXCESS-3				BCD			
b_3	b_2	b_1	b_0	g_3	g_2	g_1	g_0
0	0	0	0				
0	0	0	1				
0	0	1	0				
0	0	1	1				
0	1	0	0				
0	1	0	1				
0	1	1	0				
0	1	1	1				
1	0	0	0				
1	0	0	1				
1	0	1	0				
1	0	1	1				
1	1	0	0				
1	1	0	1				
1	1	1	0				
1	1	1	1				

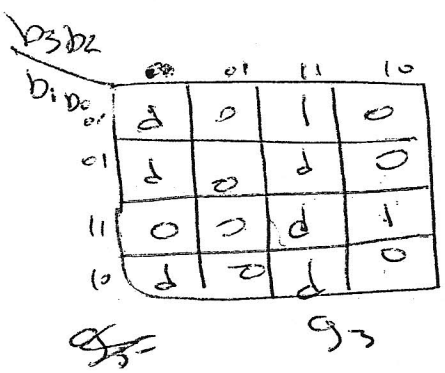
We want to design a circuit that performs the above conversion. Write the expressions of g_3, g_2, g_1, and g_0 in terms of b_3, b_2, b_1 and b_0.

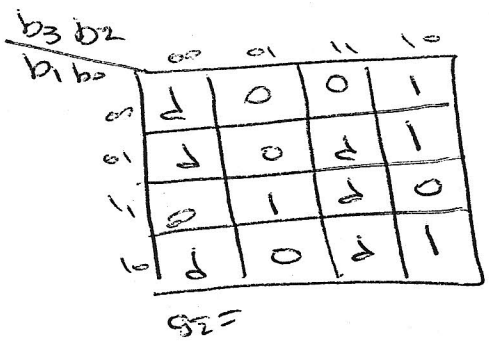
g3 = $b_3b_2 + b_3b_1b_0$

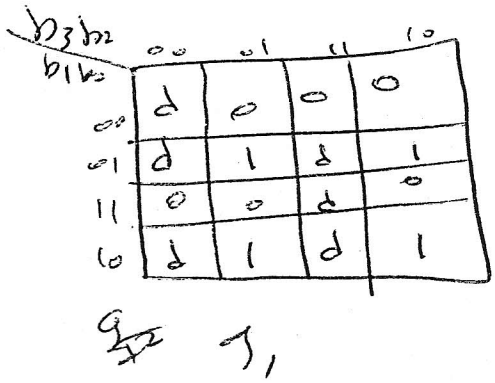
g2 = $b_2'b_1b_0 + b_2b_1'b_0' + b_2b_1b_0$ ✓

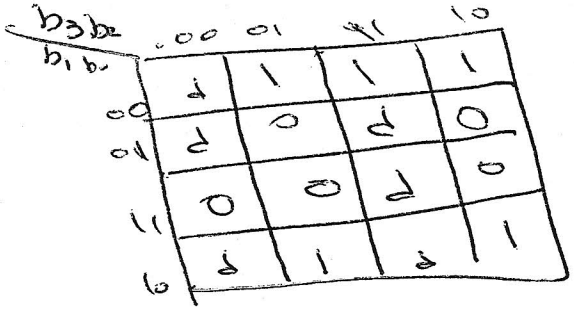
g1 = $b_1'b_0 + b_1b_0' = b_1 \oplus b_0$

g0 = b_0'



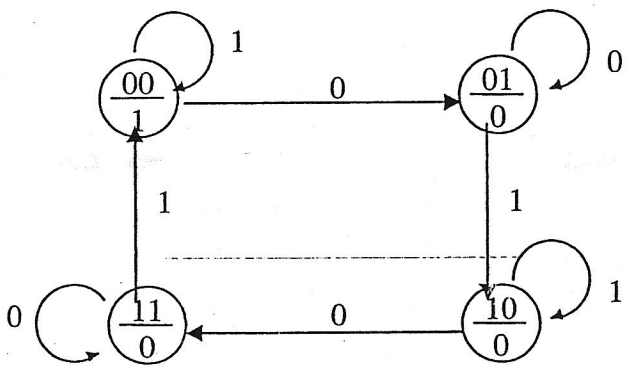






Problem 5: [10 points]

A sequential circuit has 2 flip-flops A and B, one input X and one output Y. Its state diagram is shown below. Design the circuit using D flip-flops and draw the corresponding logic diagram.



Q_A	Q_B	x = 0	x = 1	Y
0	0	01	00	1
0	1	01	10	0
1	0	11	10	0
1	1	11	00	0

$Q_A^+ ; Q_B^+$

$D_A \; D_B$

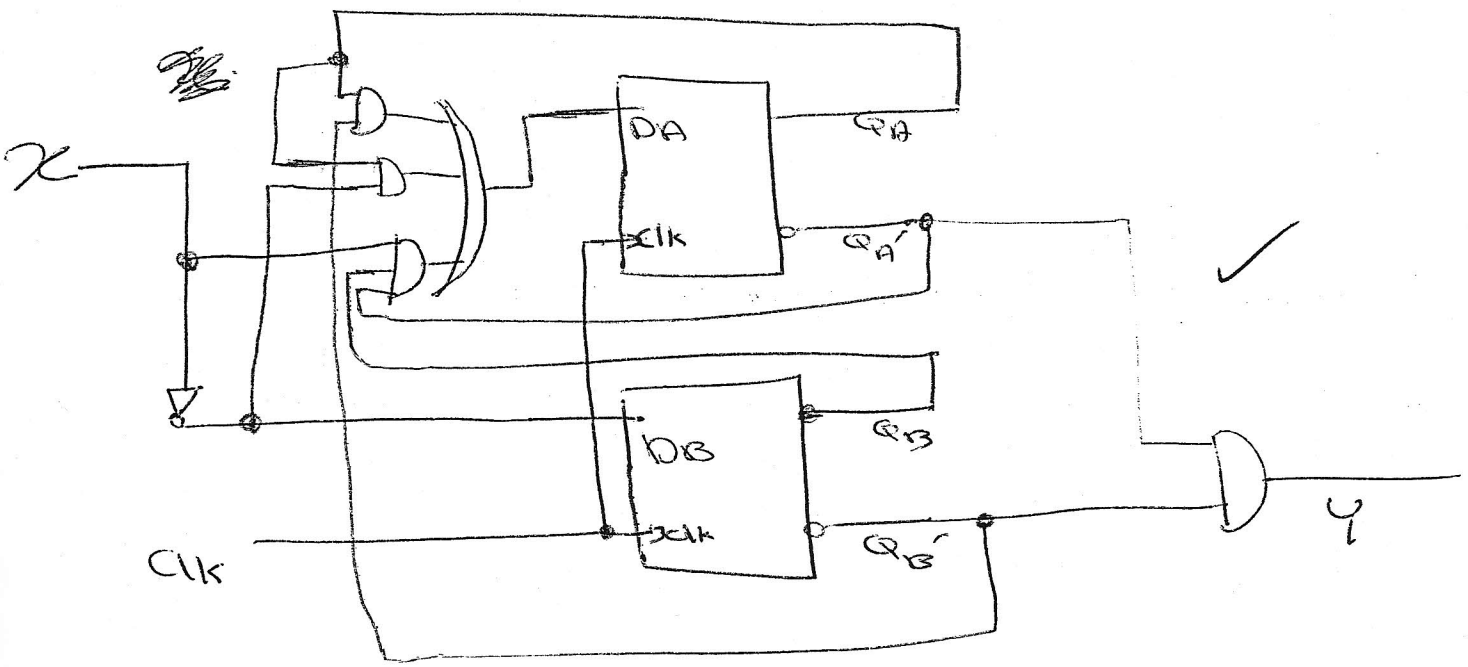
$Q_A Q_B$ \ x	00	01	11	10
0	0	0	1	1
1	0	1	0	1

$Q_A Q_B$ \ x	00	01	11	10
0	1	1	1	1
1	0	0	0	0

$D_A = Q_A Q_B' + Q_A x' + Q_A' Q_B x$

$D_B = x'$

$Y = Q_A' Q_B'$



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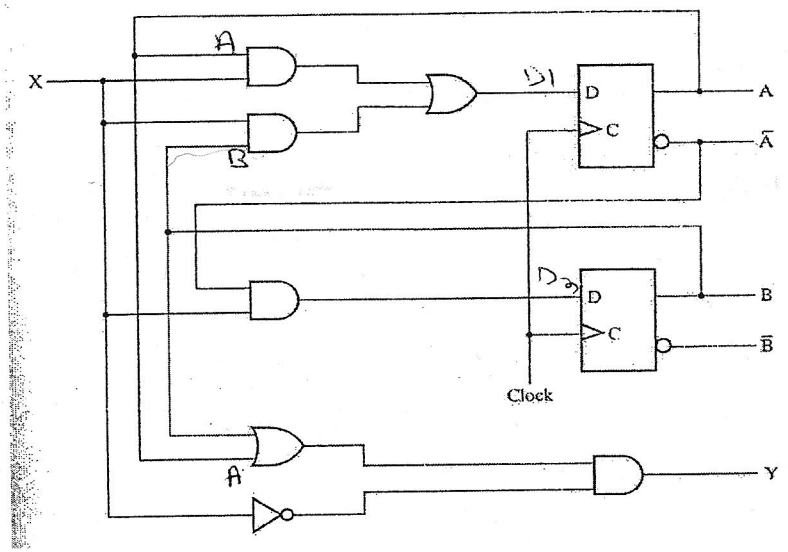
Problem 6: [10 points] 10

We would like to analyze the following clocked synchronous state machine.



A. Write the next state equations for A and B, and output Y. **[4 points]**

A* = $xA + Bx$ or $x(A+B)$ ✓ Y = $x' \cdot (A+B)$ ✓

B* = xA' ✓

B. Complete the **excitation/transition table**, and the **state table** (use the following state names A = 00, B = 01, C = 11, D = 10) **[4 points]**

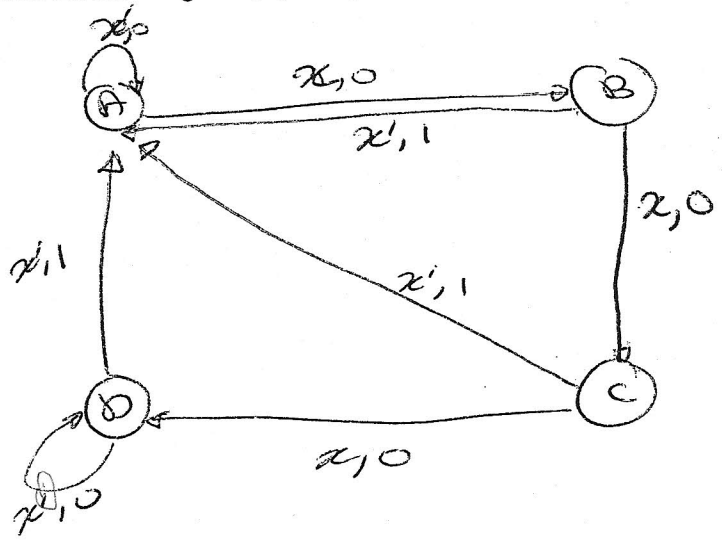
	X	
AB	**0**	**1**
00	00,0	01,0
01	00,1	11,0
11	00,1	10,0
10	00,1	10,0
	A*B*, Y	

✓

	X	
S	**0**	**1**
A	A,0	B,0
B	A,1	C,0
C	A,1	D,0
D	A,1	D,0
	S*, Y	

✓

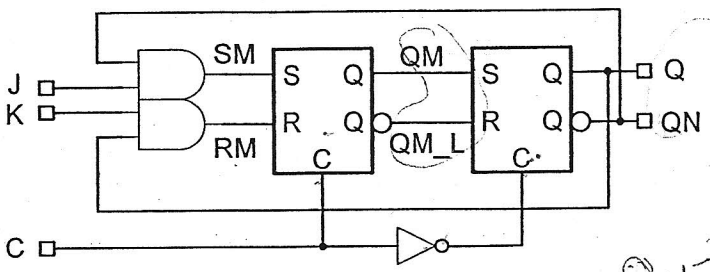
C. Draw the state diagram. **[2 points]**

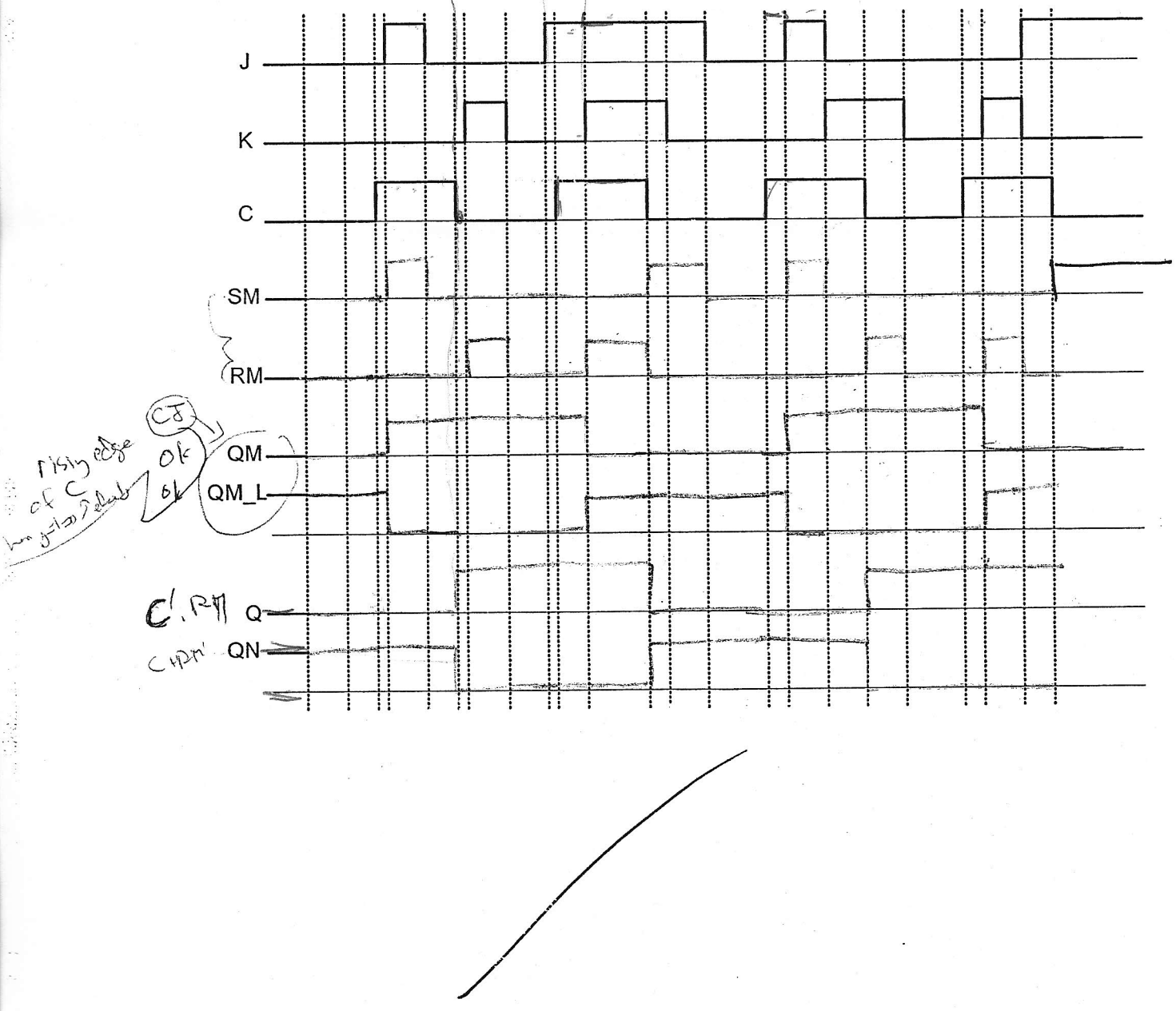


Problem 7 [10 points]

Consider the following Master-Slave JK flip-flop built using SR latches. The S input in the SR latches corresponds to a SET, the R input corresponds to a RESET, and the C input corresponds to ENABLE.

(a) Complete the timing diagram below. **[8 points]**
(b) Do you see a potential problem in this JK flip-flop? **[2 points]**





Problem 8: [10 points] 8

An *MN* flip-flop has four operations: clear to 0, no change, toggle, and set to 1, when inputs *M* and *N* are 00, 01, 10, and 11, respectively.

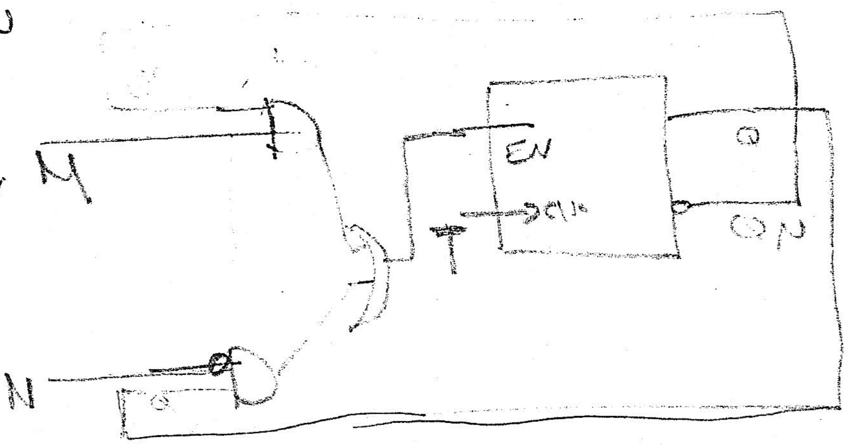
a) Determine the characteristic equation of an *MN* flip-flop. [2 points]

M	N	Q	QN
0	0	0	0
0	1	lastQ	lastQN
1	0	lastQN	lastQ
1	1	1	1

$Q = MQ' + NQ$ ✓

b) Design an *MN* flip-flop using a T flip-flop with enable and extra logic gates. [4 points]

M	N	EN
0	0	Q
0	1	0
1	0	1
1	1	Q'



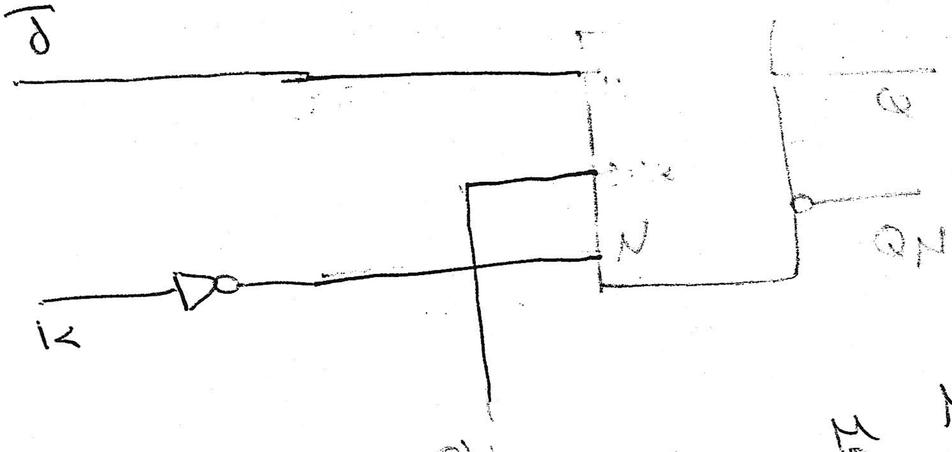
✓

c) Design a *JK* flip-flop using an *MN* flip-flop and extra logic gates. [4 points]

$Q = JQ' + K'Q$ $\quad Q = MQ' + NQ$

$\Rightarrow N = K'$

2



J	K	Q	QN
0	0	lastQ	lastQN
0	1	0	1
1	0	1	0
1	1	lastQN	lastQ

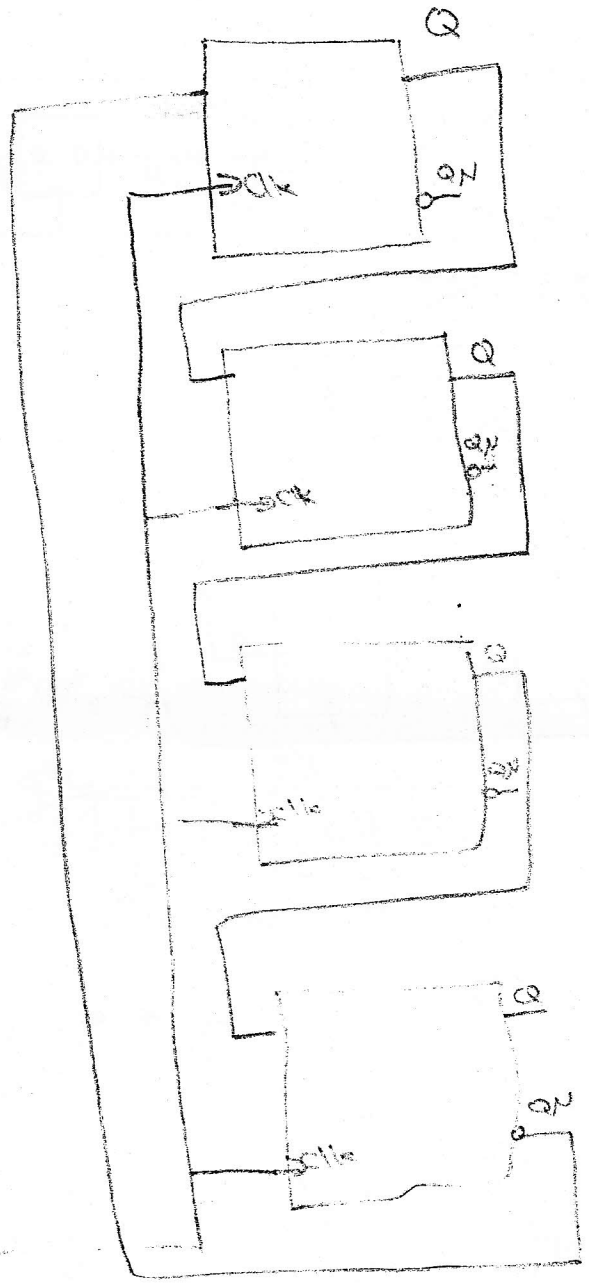
$\Rightarrow$ M: 0, Q', Q', 1 N: 1, Q, Q, 0

then you draw the diagram

Problem 9: **[10 points]** 5

Design a 4-bit Johnson counter using D flip-flops.

Answer:

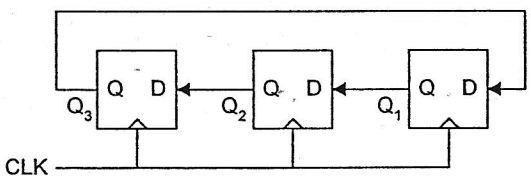


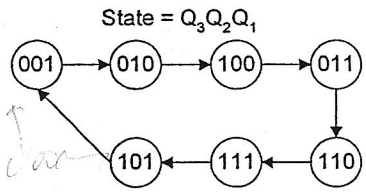
put the table used

Problem 10: [10 points]

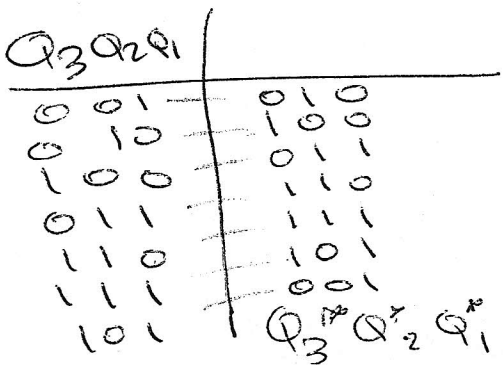
In this problem, we want to design a 3-bit counter using a shift register.

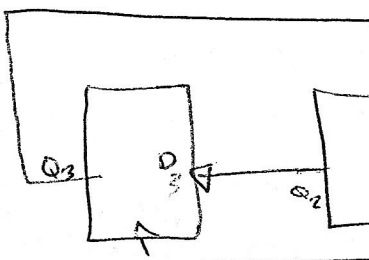
a) Assume the shift register below initially stores $Q_3Q_2Q_1$=001. Modify the shift register by adding extra logic gates so that it implements the state diagram shown on the right. (**Hint**: write next-state equations for Q_3, Q_2, Q_1).





Solution:

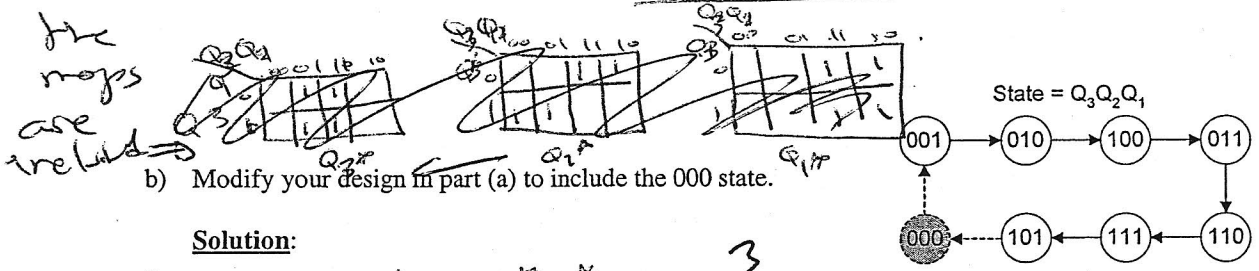




$D_3 = Q_2$

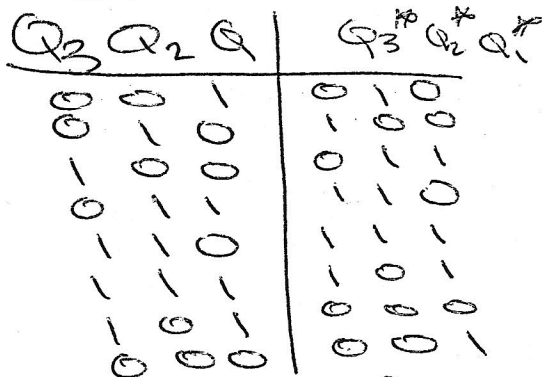
$D_2 = Q_3Q_1' + Q_3'Q_1$

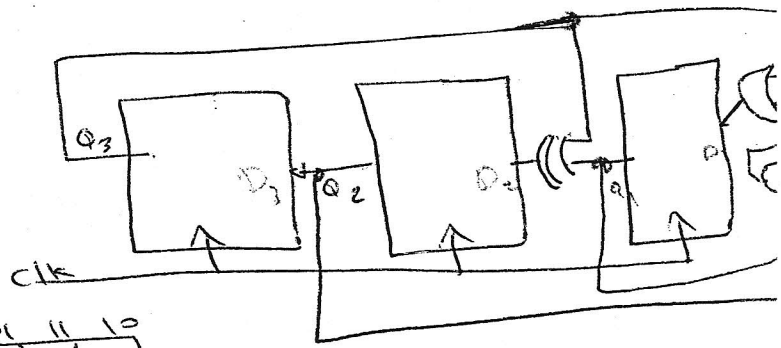
$D_1 = Q_3$

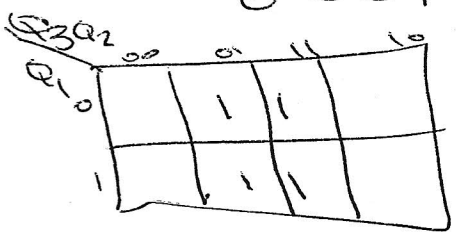


b) Modify your design in part (a) to include the 000 state.

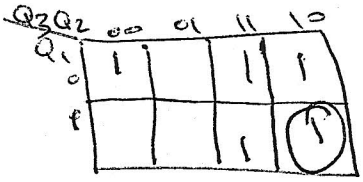
Solution:



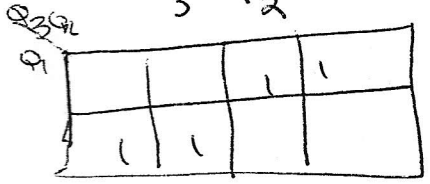




$D_3 = Q_2$



$D_1 = Q_3 + Q_2'Q_1'$



c) The counter you designed in part (b) is shown below as a black box that produces the sequence 000, 001, 010, 100, 011, 110, 111, 101 and then repeats. Describe what you would add to your counter so that it produces the sequence 000, 001, 010, 011, 100, 101, 110, 111 and then repeats.